2815

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

#5/Election

BQ 1/8/99

In Re Application of:

Shigeru ATSUMI

Serial No.: 09/028,276

Filed: February 24, 1998

For: SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND FLASH EEPROM

Group Art Unit: 2815

Examiner: J. Fenty

Attorney Docket No. 1701.73982

RESPONSE TO RESTRICTION REQUIREMENT

The Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

This paper is responsive to the office action mailed December 7, 1998 (paper no. 4), in connection with the above-identified patent application and is filed prior to the expiration of the thirty (30) day period for response set therein.

In response, Applicant elects, without traverse, the invention of Group I, i.e., claims 4-9 and 13-14; an interface circuit which may include an input buffer circuit, an output buffer circuit, and/or a level shifter. Applicant reserves the right to file a divisional application directed to the subject matter of the non-elected claims prior to the termination of proceedings in this patent application.

No fee is believed to be associated with the filing of this paper. Nonetheless, should the Patent Office determine that a fee is required, authorization is given to charge our Deposit Account No. 19-0733.

Respectfully submitted,

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